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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Appl. No.	:	10/073,550
Applicant	:	Gabriela Brase, Gregoire Grandremy
Filed	:	February 11, 2002
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Examiner	:	Duy Vu Nguyen Deo
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Docket No.	:	Z&P-INFN10176
Customer No.	:	24131

R E S P O N S E:

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Commissioner for Patents
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Alexandria, VA 22313-1450

Examiner:

The following remarks respond to the Office action dated September 4, 2003.

Reconsideration of the application is requested. Claims 1-14 remain in the application.

In item 2 of the Office action, the Examiner rejected claims 1, 5, and 7 as being fully anticipated by Havemann et al. (U.S. 6,358,849) under 35 U.S.C. § 102(e). As will be explained below, the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, a brief review of the invention as claimed is provided. Claim 1 calls for, *inter alia*, a method that includes the following steps:

> providing a semiconductor structure with functional elements formed in a substrate, a dielectric disposed on the substrate, a photoresist etching mask above the dielectric, and a polymer intermediate layer between the etching mask and the dielectric layer;
>
> etching the dielectric layer and the polymer intermediate layer for the dual damascene patterning with a CF_4 ARC open process with high selectivity with respect to the photoresist of the etching mask. (Emphasis added by Applicants.)

Claims 1 and 9 of the instant application are directed to methods for structuring an oxide layer on a substrate during a double damascene patterning process. Such patterning during double damascene processes is usually carried out using a photoresist in combination with an ARC layer. These two layers are used to structure an oxide layer positioned underneath the ARC and photoresist layer. The use of an

polymer ARC layer in such double damascene processes leads to the problem of deposition of ARC polymer in the contact holes that have previously been opened. *See* specification, page 5, lines 12 to 22. This deposition leads to the formation of so-called "fences" around the contact holes. In turn, fences make the subsequent metallization step more difficult or lead to internal stresses in the semiconductor element, proceeding from said fences. *See* specification, page 6, lines 1 to 5.

The prior art has suggested to reduce the formation of fences by reducing sidewall deposition of polymer during the etching of the interconnect by increasing the addition of oxygen to the etchant. However, this diminishes selectivity towards the photoresist and reduces resolution of the etchant process, i.e. the critical dimension is widened. *See* specification, page 6, lines 7 to 16.

The present invention solves these problems connected to the use of polymer intermediate layers (ARC-layers) by using a highly selective CF_4-ARC open process for etching both the polymer intermediate layer and the oxide layer positioned underneath said ARC-layer. This process etches any polymer present in the interconnect at the same time as the oxide so that no fence formation can take place. *See* specification, page 9, lines 8 to 17.

In contrast, Havemann et al. (US 6,358,849) describes a dual damascene process using a siliconoxynitride-ARC (SiON-ARC). *See* column 3, line 17 to 18 and lines 66 to 67. This is not a polymer ARC, but an inorganic ARC. The problem of polymer deposition during the oxide etch and fence formation caused by this organic polymer deposition is not encountered with such an inorganic ARC.

Consequently, the methods according to independent claims 1 and 9 of the present invention are novel over the art disclosed by Havemann et al. Furthermore, the methods according to the present invention would not be obvious to one with ordinary skill in the art viewing Havemann et al. Not only do Havemann et al. fail to disclose the use of a polymer intermediate layer used as an ARC during the etching of the respective oxide layer, Havemann et al. also use a completely different approach for avoiding problems connected with the presence of interconnects which have already been opened. As becomes apparent from Figures 1h to 1j, in the dual damascene method described by Havemann et al., an interconnect is etched through layers 170, 171 172 and 173; *see* column 3, line 61 to column 4, line 12. This interconnect is then filled with a temporary filler made of parylene (*see* column 4, line 8 to 12). This filler remains in the interconnect during the subsequent formation of trenches 180 and is only then reopened

with an oxygen plasma (*see* column 4, lines 27 to 31) before metallization.

Therefore, the method described by Havemann is completely different from the method of the present invention. Therefore, one with ordinary skill in the art would be given no incentive by this reference to use a polymer intermediate ARC layer instead of an inorganic siliconoxynitride ARC layer.

In item 4 of the Office action, the Examiner rejected claims 3, 4, 6, 8, and 9-13 as being unpatentable over Khajehnouri et al. (U.S. 6,117,786) under 35 U.S.C. § 103(a). Khajehnouri et al. only describes an etching process for etching an oxide layer during which polymer deposition is controlled in such a manner that anisotropically etched openings are obtained and etch stop is avoided. Dual damascene processes or the use of polymer intermediate layers (ARC) during oxide etch are not mentioned in this reference. Consequently, the method of the present invention is not made obvious by Havemann et al. in view of Khajehnouri et al.

In view of the foregoing, reconsideration and allowance of claims 1-14 are solicited. In the event the Examiner should still find any of the claims to be unpatentable, please telephone counsel so that patentable language can be substituted.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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